

Modulation Extension Control of Hybrid Cascaded H-bridge Multilevel Converters with 7-level Fundamental Frequency Switching Scheme

Zhong Du, Burak Ozpineci, and Leon M. Tolbert
Power Electronics and Electric Machinery Research Center
National Transportation Research Center
Oak Ridge National Laboratory
2360 Cherahala Boulevard
Knoxville, TN 37932, USA

Abstract—This paper presents a modulation extension control algorithm for hybrid cascaded H-bridge multilevel converters. The hybrid cascaded H-bridge multilevel motor drive using only a single dc source for each phase is promising for high-power motor drive applications since it can greatly decrease the number of required dc power supplies, has high-quality output power because of its high number of output levels, and has high conversion efficiency and low thermal stress because it uses a fundamental frequency switching scheme. However, one disadvantage of the 7-level fundamental frequency switching scheme is that its modulation index range is too narrow when the capacitor's voltage balance is maintained. The proposed modulation extension control algorithm can greatly increase the capacitors' charging time and decrease their discharging time by injecting triplen harmonics to extend the modulation index range of the hybrid cascaded H-bridge multilevel converters to conquer this problem. Therefore, the proposed modulation extension control algorithm has not only a wider modulation index range but also all the advantages of inherent high output power quality, low output switching frequency and high conversion efficiency, and high-speed capability.

I. INTRODUCTION

The multilevel converter is a promising power electronics topology for high-power motor drive applications because of its low electromagnetic interference (EMI) and high efficiency with a low-frequency control method [1–5]. Among the multilevel converter topologies, the cascaded multilevel converter with separate dc sources closely fits the needs of all-electric vehicles because it can use the onboard batteries or fuel cells to generate a sinusoidal voltage waveform to drive the main vehicle traction motor.

Traditionally, each phase of a cascaded multilevel converter requires n dc sources for $2n + 1$ levels. For many applications, to get many separate dc sources is difficult, and having too many dc sources will require many long cables and could lead to voltage unbalance among the sources. To reduce the number of dc sources required when the cascaded H-bridge multilevel converter is applied to a motor drive, a hybrid cascaded multilevel converter has been proposed which only uses a single dc source for each phase. This hybrid cascaded multilevel converter has the advantages of higher speeds with a low switching frequency (especially useful for electric/hybrid electric vehicle applications), which offers inherent low switching losses and high conversion efficiency [6–7]. However, a disadvantage of the hybrid cascaded multilevel converter is that it has a narrow modulation index range when a 7-level fundamental frequency switching scheme is used, and this disadvantage limits its highest output voltage when maintaining the capacitors' voltages. To conquer this problem, this paper proposes a modulation extension control algorithm to extend the modulation index range for hybrid cascaded H-bridge multilevel converters. The reason for a narrow modulation index range is the longer discharging time and shorter charging time when the hybrid cascaded multilevel converters output high 7-level voltages. The proposed modulation extension control algorithm can greatly increase the capacitors' charging time and decrease their discharging time by injecting triplen harmonics to extend the modulation index range of the hybrid cascaded H-bridge multilevel converters to conquer this problem. Therefore, the proposed modulation extension control algorithm has not only a wider modulation index range but also all the advantages of inherent high output power quality, low output switching frequency, high conversion efficiency, and high-speed capability. This control scheme is especially suitable for fuel cell vehicle motor drive applications. Simulation and experiments verified the proposed control algorithm with the desired features.

Prepared by the Oak Ridge National Laboratory, Oak Ridge, Tennessee 37831, managed by UT-Battelle for the U.S. Department of Energy under contract DE-AC05-00OR22725.

The submitted manuscript has been authored by a contractor of the U.S. Government under Contract No. DE-AC05-00OR22725. Accordingly, the U.S. Government retains a non-exclusive, royalty-free license to publish from the contribution, or allow others to do so, for U.S. Government purposes.

II. CONTROL OF HYBRID CASCADED H-BRIDGE MULTILEVEL CONVERTER WITH 7-LEVEL OUTPUT VOLTAGE

A 7-level hybrid cascaded H-bridge multilevel converter has two H-bridges for each phase. One H-bridge is connected to a dc source and another is connected to a capacitor, as shown in Fig. 1. The dc source for the first H-bridge (H_1) could be a battery or fuel cell with an output voltage of V_{dc} , and the dc source for the second H-bridge (H_2) is the capacitor voltage, to be held at V_c . The output voltage of the first H-bridge is denoted by v_1 , and the output of the second H-bridge is denoted by v_2 so that the output voltage of the cascaded multilevel converter is

$$v(t) = v_1(t) + v_2(t) \quad (1)$$

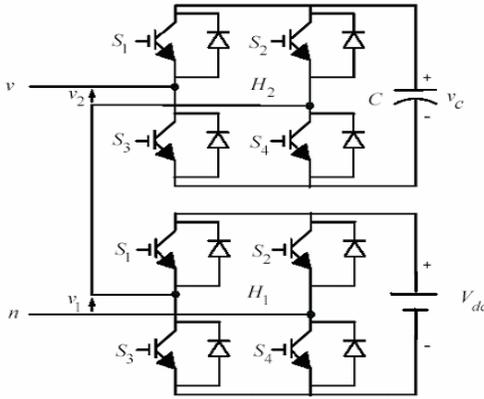


Fig. 1. Topology of a single phase of the proposed multilevel converter with a single dc source for the first level and capacitors for other levels.

By opening and closing the switches of H_1 appropriately, the output voltage v_1 can be made equal to $-V_{dc}$, 0, or V_{dc} while the output voltage of H_2 can be made equal to $-V_c$, 0, or V_c by opening and closing its switches appropriately. Therefore, the output voltage of the converter is a combination of V_{dc} and V_c which can have nine possible values $-(V_{dc}+V_c)$, $-V_{dc}$, $-(V_{dc}-V_c)$, $-V_c$, 0, V_c , $(V_{dc}-V_c)$, V_{dc} , $(V_{dc}+V_c)$.

To regulate the capacitor's voltage to guarantee the output power quality, a 7-level fundamental switching scheme has been proposed. This switching scheme uses a possible cycle to output $-(V_{dc}+V_c)$, $-V_{dc}$, $-(V_{dc}-V_c)$, 0, $(V_{dc}-V_c)$, V_{dc} , $(V_{dc}+V_c)$ voltage levels; and the dc source is charging the capacitor simultaneously when output is $-(V_{dc}-V_c)$ and $(V_{dc}-V_c)$, which is called a charging cycle. Similarly, the switching scheme uses another possible cycle to output $-(V_{dc}+V_c)$, $-V_{dc}$, $-V_c$, 0, V_c , V_{dc} , $(V_{dc}+V_c)$ voltage levels; and the capacitor can be discharged simultaneously, which is called a discharging cycle. Then the capacitors' voltage can be regulated by charging and discharging when the multilevel converter is running. When $V_c = V_{dc}/2$ is chosen, the output voltage waveform is a 7-level waveform. Although the power width modulation (PWM) control method is popular for inverters regardless of their topologies [8–13], 7-level fundamental frequency switching

control is a good method for the hybrid cascaded H-bridge multilevel converter, which is shown in Fig. 2. This switching scheme uses three switching angles θ_1 , θ_2 , and θ_3 to output a voltage waveform and to eliminate the low-order 5th and 7th harmonics [14–17]. The solutions of the switching angles can be found by many methods [18–21], such as the resultant method [18–19]. For the 7-level hybrid cascaded H-bridge motor drive control, the output voltage can be represented by the mathematical model

$$V(\omega t) = \sum_{n=1,3,5\dots}^{\infty} \frac{4V_{dc}}{n\pi} (\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3)) \sin(n\omega t) \quad (2)$$

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = m$$

$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0$$

$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) = 0$$

For convenience, here the modulation index is defined as

$$m = \frac{\pi V_1}{2V_{dc}} \quad (3)$$

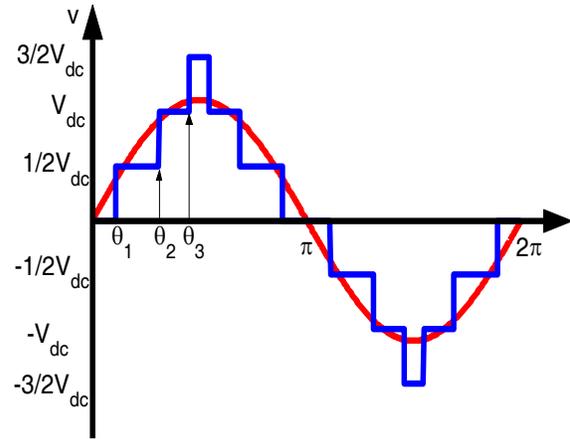


Fig. 2. 7-level equal step output voltage waveform.

From Fig. 2, it can be seen that the capacitor is discharging when the inverter outputs voltage $-(V_{dc}+V_c)$ and $(V_{dc}+V_c)$ regardless of charging cycle or discharging cycle. During a cycle, if the discharging amount is greater than the charging amount, then the capacitor's voltage balance is not possible. For a high modulation index range of 7-level fundamental frequency switching control, the discharging amount is greater than the charging amount, which renders the capacitor's voltage regulation control impossible.

In addition, the charging amount and discharging amount are related to the power factor angle. This can be seen from Fig. 3, which shows the charging and discharging situation with different power factor angles (lead or lag).

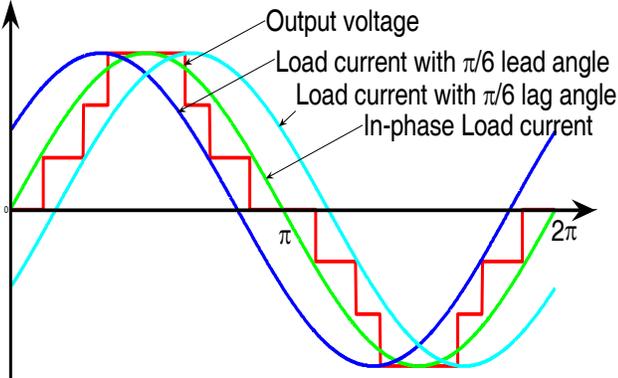


Fig. 3. Capacitor charging and discharging time with different load current without triplen harmonic voltage compensation.

III. MODULATION INDEX EXTENSION CONTROL BY INJECTING TRIPLEN HARMONICS

To decrease the discharging time and increase the charging time, a new modulation extension control method of injecting triplen harmonic voltages into the 7-level output voltage is proposed. A triplen harmonic which can be represented by

$$V_{tri}(\omega t) = \sum_{n=1,3,5,\dots}^{\infty} \frac{4V_{dc}}{n\pi} \cos(n\theta_3) \sin(3n\omega t) \quad (4)$$

is injected into the 7-level output voltage, and the output voltage waveform is changed (shown in Fig. 4). The triplen harmonic voltages will automatically cancel in the line-line voltages and will not change the fundamental frequency contents. Therefore, here, the only effect is to change the charging period and discharging period. From Fig. 5, it can be seen that the original long discharging period has been changed into two short discharging periods.

To analyze the voltage balance situation due to capacitor charging and discharging in detail, define the charging amount

$$Q_{charging} = \int_0^{2\pi} I_{charging} d\theta \quad (5)$$

and discharging amount

$$Q_{discharging} = \int_0^{2\pi} I_{discharging} d\theta \quad (6)$$

Then in a whole cycle, the net accumulation amount is defined as

$$Q_{accumulation} = Q_{charging} - Q_{discharging} \quad (7)$$

Therefore, if capacitor voltage balance is possible, then the net accumulation amount must be greater than zero in a whole cycle. Based on this analysis, the net accumulation amount is calculated for the 7-level output voltage cases with and without the triplen harmonic compensation method.

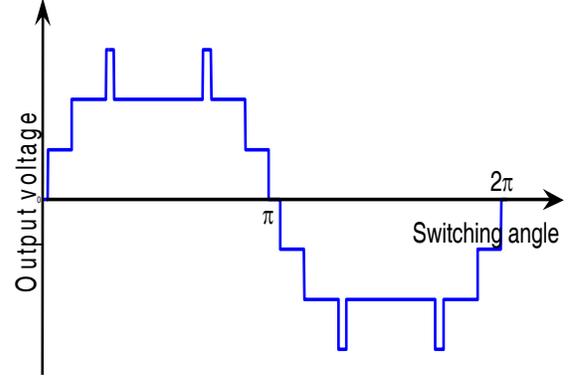


Fig. 4. Output voltage waveform with triplen harmonic compensation.

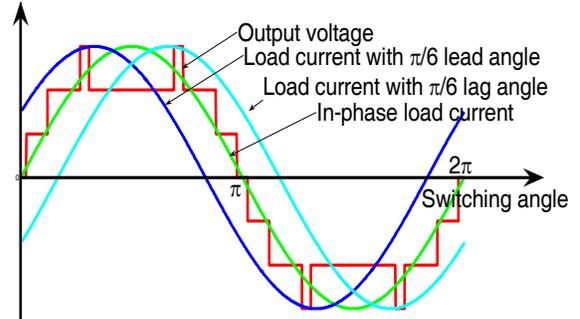


Fig. 5. Capacitor charging and discharging time with different load current with triplen harmonic voltage compensation.

If only a 7-level fundamental frequency switching scheme is used to regulate the capacitor's voltage, the accumulation curve is shown in Fig. 6. The highest modulation index that can balance the capacitor's voltage is around 1.54.

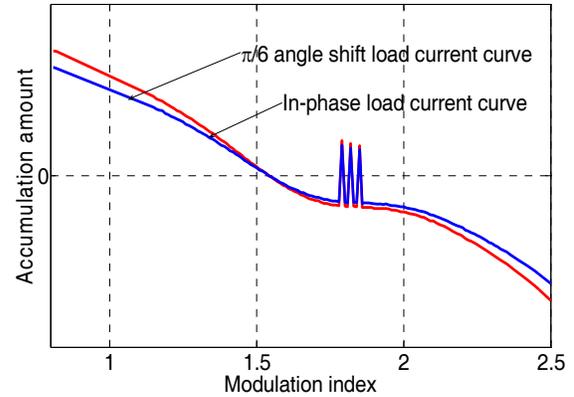


Fig. 6. Accumulation curve without triplen harmonic voltage compensation.

If the triplen harmonic voltage compensation method is used, the accumulation curve is shown in Fig. 7. The highest modulation index that can balance the capacitor's voltage is around 2.

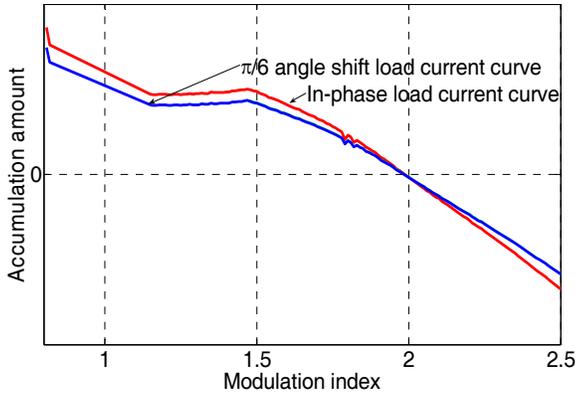


Fig. 7. Accumulation curve with triplen harmonic voltage compensation.

If Figs. 6 and Fig. 7 are compared, it can be seen that the triplen harmonic compensation method can increase the modulation index range by 33% for a hybrid cascaded H-bridge multilevel converter to balance the capacitors' voltage.

IV. EXPERIMENT IMPLEMENTATION AND VALIDATION

To experimentally validate the proposed hybrid cascaded H-bridge multilevel motor drive control scheme, a prototype three-phase cascaded H-bridge multilevel converter has been built using metal oxide semiconductor field effect transistors (MOSFETs) as the switching devices (Fig. 8). Three 48-V dc power supplies (one for each phase) feed the motor drive. A real-time variable-output voltage, variable-frequency three-phase motor drive controller based on an Altera FLEX 10K field programmable gate array (FPGA) is used to implement the control algorithm. For convenience of operation, the FPGA controller is designed as a card to be plugged into a personal computer, which uses a peripheral component interconnect (PCI) bus to communicate with the microcomputer. The FPGA controller board will be based on a PCI bus. To maintain the capacitor's voltage balance, a voltage sensor is used to detect the capacitor's voltage and feed the voltage signal into the FPGA controller. A 1-kW induction motor is used as the load of the inverter.

To verify the proposed voltage balance control algorithm, the modulation index $m=1.97$ is chosen for the experiment. The phase voltage waveform and phase current waveform are shown in Fig. 9. The experiment shows that the capacitor's voltage can be regulated at 24 V, which is half of the dc source voltage.

Fig.10 shows the normalized fast Fourier transform (FFT) analysis of the phase voltage, and Fig. 11 shows the normalized FFT analysis of the phase current. From the voltage spectrum distribution in Fig. 10, it can be seen that the 5th and 7th harmonic voltages are near zero and the triplen harmonic voltages (such as the 3rd, 9th etc.) are not zero. From the current spectrum distribution shown in Fig. 11, it also can be seen that it has no 5th or 7th current harmonics, no triplen current harmonics.



Fig. 8. The 10-kW multilevel inverter prototype.

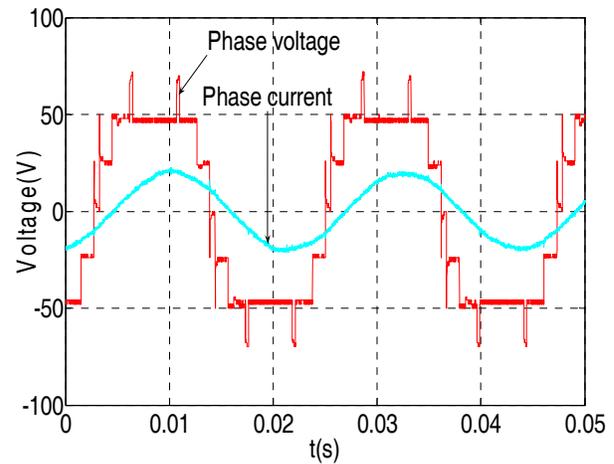


Fig. 9. Experimental voltage and current waveforms with a motor load and regulated capacitor's voltage.

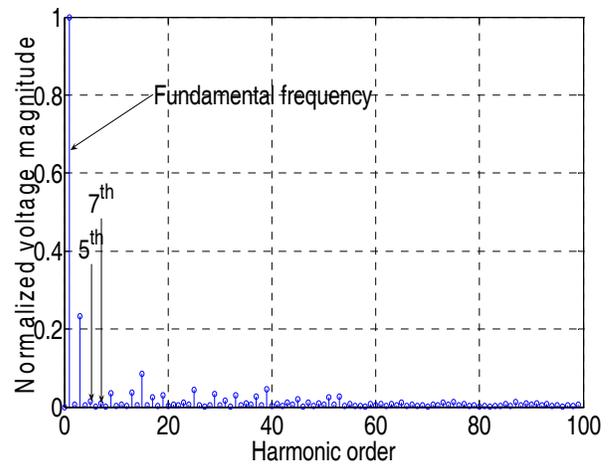


Fig. 10. Normalized FFT analysis of phase voltage shown in Fig. 9.

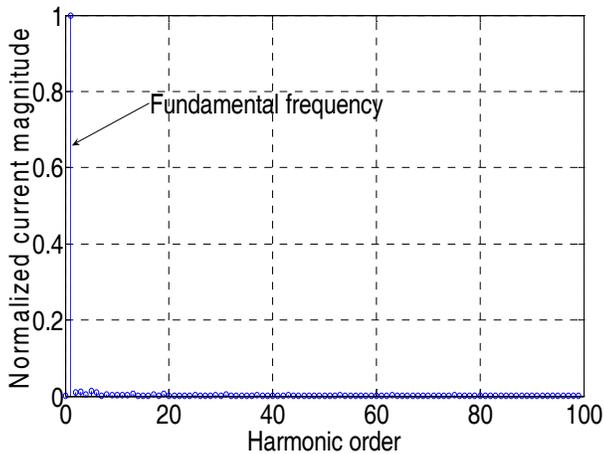


Fig. 11. Normalized FFT analysis of phase current shown in Fig. 9.

Further experiments show that for a high modulation index range, a 7-level output voltage waveform with triplen harmonic compensation can balance the capacitors' voltages; but a 7-level output voltage waveform without triplen harmonic compensation cannot balance the capacitors' voltages.

In theory, the voltage balance can reach a modulation index $m=2.0$. For actual experiments, though, because of the switching loss, the conduction loss of the switching devices, and the wire copper loss of the circuit, the modulation index for the capacitor's voltage balance is a little less than 2.0. In the experiments, if the modulation index is higher than 1.97, it is shown that the capacitor's voltage is maintained at a lower voltage instead of half of the dc source voltage.

V. CONCLUSIONS

This paper proposed a new modulation extension control algorithm for 7-level hybrid cascaded H-bridge multilevel converters that use only one power source for each phase to balance the capacitors' voltages while producing the desired 7-level voltage waveforms. It can be derived from the simulation and experiment results that this control algorithm can balance the capacitors' voltages while producing higher fundamental voltages with specific low-order harmonics eliminated. This control method can effectively extend the modulation range to output a higher fundamental frequency voltage compared with the traditional 7-level fundamental frequency switching scheme. It is promising for high-power motor drive applications.

ACKNOWLEDGMENT

The authors would like to thank the National Transportation Research center of Oak Ridge National Laboratory for support of this research.

REFERENCES

- [1] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. on Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.
- [2] J. S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," *IEEE Trans. on Ind. Appl.*, vol. 32, no.3, pp. 509–517, May/June 1996.
- [3] J. Rodríguez, J. Lai, and F. Peng, "Multilevel inverters: a survey of topologies, controls and applications," *IEEE Trans. on Ind. Appl.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [4] P. Hammond, "A new approach to enhance power quality for medium voltage ac drives," *IEEE Trans. on Ind. Appl.*, vol. 33, pp. 202–208, Jan./Feb. 1997.
- [5] W. A. Hill and C. D. Harbourt, "Performance of medium voltage multilevel inverters," *IEEE Industry Applications Society Annual Meeting*, October 1999, Phoenix, AZ, pp. 1186–1192.
- [6] Zhong Du, L. M. Tolbert, J. N. Chiasson, B. Ozpineci, Li Hui, A. Q. Huang, "Hybrid cascaded H-bridges multilevel motor drive control for electric vehicles," *IEEE Power Electronics Specialists Conference*, June, 18–22, 2006, Jju, Korea, pp. 1–6.
- [7] Z. Du, L. M. Tolbert, J. N. Chiasson, "A cascade multilevel inverter using a single fuel cell DC source," *IEEE Applied Power Electronics Conference*, March 6–10, 2006, Dallas, TX, vol. 1, pp. 419–423.
- [8] G. Carrara, S. Gardella, M. Marchesoni, R. Salutati, and G. Sciuotto, "A new multilevel PWM method: A theoretical analysis," *IEEE Trans. on Power Electronics*, vol. 7, no. 3, pp. 497–505, July 1992.
- [9] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel PWM methods at low modulation indices," *IEEE Trans. on Power Electronics*, vol. 15, no. 4, pp. 719–725, July 2000.
- [10] L. M. Tolbert and T. G. Habetler, "Novel multilevel inverter carrier-based PWM method," *IEEE Trans. on Ind. Appl.*, vol. 35, no. 5, pp. 1098–1107, Sept./Oct. 1999.
- [11] J. Vassallo, J. C. Clare, and P. W. Wheeler, "A power-equalized harmonic-elimination scheme for utility-connected cascaded H-bridge multilevel converters," *IEEE Industrial Electronics Society Annual Conference*, Nov. 2–6, 2003, pp. 1185–1190.
- [12] S. Sirisukprasert, J.-S. Lai, and T.-H. Liu, "Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters," *IEEE Trans. on Ind. Appl.*, vol. 49, no. 4, pp. 875–881, Aug. 2002.
- [13] P. C. Loh, D. G. Holmes, and T. A. Lipo, "Implementation and control of distributed PWM cascaded multilevel inverters with minimum harmonic distortion and common-mode voltages," *IEEE Trans. on Power Electronics*, vol. 20, no. 1, pp. 90–99, Jan. 2005.
- [14] H. S. Patel and R. G. Hoft, "Generalized harmonic elimination and voltage control in thyristor inverters: Part I—harmonic elimination," *IEEE Trans. on Ind. Appl.*, vol. 9, pp. 310–317, May/June 1973.
- [15] H. S. Patel and R. G. Hoft, "Generalized harmonic elimination and voltage control in thyristor inverters: Part II—Voltage control technique," *IEEE Trans. on Ind. Appl.*, vol. 10, pp. 666–673, Sept./Oct. 1974.
- [16] P. N. Enjeti, P. D. Ziogas, and J. F. Lindsay, "Programmed PWM techniques to eliminate harmonics: A critical evaluation," *IEEE Trans. on Ind. Appl.*, vol. 26, no. 2, pp. 302–316, March/April. 1990.
- [17] Z. Du, L. M. Tolbert, and J. N. Chiasson, "Active harmonic elimination for multilevel converters," *IEEE Trans. on Power Electronics*, vol. 21, no. 2, pp. 459–469, March 2006.
- [18] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Z. Du, "Control of a multilevel converter using resultant theory," *IEEE Trans. on Control System Theory*, vol. 11, no. 3, pp. 345–354, May 2003.
- [19] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Z. Du, "A new approach to solving the harmonic elimination equations for a multilevel converter," *IEEE Industry Applications Society Annual Meeting*, October 12–16, 2003, Salt Lake City, Utah, pp. 640–645.
- [20] Z. Du, L. M. Tolbert, and J. N. Chiasson, "Modulation extension control for multilevel converters using triplen harmonic injection with low switching frequency," *IEEE Applied Power Electronics Conference*, March 6–10, 2004, Austin, TX, pp. 419–423.
- [21] T. Kato, "Sequential homotopy-based computation of multiple solutions for selected harmonic elimination in PWM inverters," *IEEE Trans. on Circuits and Systems I*, vol. 46, no. 5, pp. 586–593, May 1999.